



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---------------------------------|-------------|----------------------|---------------------|------------------|
| 10/550,899 | 09/27/2005 | Dong-Gyu Kim | AB-1521 US | 4096 |
| 32605 | 7590 | 02/06/2009 | EXAMINER | |
| MACPHERSON KWOK CHEN & HEID LLP | | | HEYMAN, JOHN S | |
| 2033 GATEWAY PLACE | | | | |
| SUITE 400 | | | ART UNIT | PAPER NUMBER |
| SAN JOSE, CA 95110 | | | 2871 | |
| | | | | |
| | | | MAIL DATE | DELIVERY MODE |
| | | | 02/06/2009 | PAPER |

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

| | | | |
|------------------------------|------------------------|---------------------|--|
| Office Action Summary | Application No. | Applicant(s) | |
| | 10/550,899 | KIM, DONG-GYU | |
| | Examiner | Art Unit | |
| | JOHN HEYMAN | 2871 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 08 September 2008.
- 2a) This action is **FINAL**. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-3,5,6,9-11 and 13-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-3, 5, 6, 9-11, 13-27 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ . |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ . | 6) <input type="checkbox"/> Other: _____ . |

DETAILED ACTION

1. In view of the amendments to these claims, the rejection based on the references Chung (US 6,870,187) and Yamamoto (US 2002/0182766) have been overcome and are hereby withdrawn. However, these claims remain unpatentable in view of an updated prior art search based on the claim amendments.
2. Claims 27 and 28 are objected to as improperly numbered. As there is no Claim 26, these claims should be re-numbered 26 and 27 respectively. Correction is required.

Claim Rejections - 35 USC § 103

3. Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okamoto et al. (Okamoto – US 2002/0140883), newly cited. Looking at the various figures of Okamoto, and comparing them with independent Claim 1, a TFT array panel comprises a gate line 8(1) (Fig. 1) formed on an insulating substrate 11 (Fig. 3) including a gate electrode 4 (Figs. 1 and 4); a gate insulating layer 13 formed on the gate line 1 (Fig. 3); a semiconductor layer 12 formed on the gate insulating layer 13 (Fig. 4); a data line 2 formed on the gate insulating layer 13 and including a source electrode 5 (Fig. 1); a drain electrode 6 formed at least in part on the semiconductor layer 12 (Fig. 4); the TFT of Fig. 4 then shows gate electrode, source electrode, drain electrode and the semiconductor layer as recited. Then, a light blocking layer 33 is provided to block light reflected from a portion of the TFT (Fig. 8) as recited; a plurality of color filters 46B,R,G formed above the TFT, wherein two of the color filters 46B and 46R are located directly above the portion of the TFT as recited (Fig. 8). Pixel electrode 10 is contacting drain electrode 6 via drain signal line 7 through contact hole 9 (Fig. 1)

as recited; a spacer 50 formed on (above) light blocking layer 33 (Fig. 8); and storage conductor 7 formed on the gate insulating layer 13, overlapping gate line 1 and electrically contacting pixel electrode 10 (Fig. 3) is shown.

4. Not shown are the color filters overlapping each other feature. However, this feature is shown in Fig. 5 of Okamoto where color filters 20 and 16 overlap each other over data line 2. It would have been obvious for the skilled worker to apply the teaching of Fig. 5 of Okamoto to the TFT of Fig. 8 therein for the reason that it is well known in the liquid crystal art that color filters may enhance the light blocking effectiveness in a liquid crystal structure as shown in the Fig. 5 embodiment of Okamoto. Thus, it would not be patentable to apply the enhanced light-shielding effectiveness of Fig. 5 directly above the TFT circuit in Fig. 8 since such is deemed a well known design expedient as taught by Fig. 5 of Okamoto under 35 USC 103.

5. Regarding Claim 5, note Fig. 3 of Okamoto in which the color filters 16 have an opening 9 exposing the storage conductor 7 at least in part for connection between the storage conductor 7 and pixel electrode 10 to thus meet this claim.

6. Claims 2, 3, 6, 9-11 and 13-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okamoto as applied to claim 1 above, and further in view of Rho et al. (Rho – US 6,862,050) cited of record. Not disclosed by Okamoto are certain details recited by the above claims.

7. Thus, regarding Claims 2, 11 and 14 Okamoto fails to disclose that the light blocking layer comprises an organic material including a black pigment as recited in

these claims. This feature is taught in Rho in col. 5, line 43 to thus render obvious this limitation in Claims 2, 11 and 14.

8. Regarding Claims 11 and 14, note that the first and second panels are met by panels 30 and 31 in Okamoto. The remaining limitations recited in these claims are as indicated in the rejection of Claim 1 above where such limitations exist. For example, Claim 14 does not recite the “storage conductor” limitation in the last clause of Claim 1, so that this limitation is ignored for Claim 14.

9. Regarding Claim 3, Okamoto fails to disclose that the spacer comprises an organic material as recited in this claim. This feature is taught by Rho in col. 8, line 25 for spacer 190 shown in Fig. 13, for example. It would have been obvious to apply the teachings of Rho to Okamoto to meet Claims 2, 3, 11 and 14 since this amounts to nothing more than applying a known technique to a known device ready for improvement to yield predictable results, *KSR International Co. v. Teleflex Inc.* 82 USPQ2d 1385 (2007), relied upon.

10. Regarding Claim 6, note storage electrode 30 formed under gate insulating layer 40 and overlapping the pixel electrode 140 shown in Fig. 3 of Rho to thus meet this claim.

11. Regarding Claim 9, note passivation layer 100 is provided over the TFT of Rho in Fig. 3, for example. The passivation layer comprises an acrylic material having a dielectric constant smaller than 4.0 (col. 5, lines 13 and 26) to thus render obvious this claim under 35 USC 103.

12. Regarding Claim 10, note semiconductor layer 80 in Rho has substantially the same planar shape as the data lines 81 and drain electrodes except for a portion between the source and drain electrodes 80 and 90 (Figs. 2 and 3) to render obvious the limitation of this claim.

13. Regarding Claims 13 and 15, note the protrusion at the end of layer 110 on the first panel in Fig. 13 of Rho which shows a height smaller than the spacer 190 and having a slanted lateral surface to thus meet these claims.

14. Regarding Claims 16-18, note that Rho discloses that passivation layer 100 is made of a flowable organic insulating material having a low dielectric constant (col. 5, line 14) that may obviously include the a-Si:C:O material recited since such is well known to have a low dielectric constant, to thus render obvious these claims.

15. Regarding Claim 19, note that spacer 50 in Okamoto (or spacer 190 in Rho) is formed between the first and second panels to thus meet this claim.

16. Regarding Claims 20-22, note that light blocking layer 110 in Rho is formed above the data line 81 (Fig. 2, for example) to thus meet these claims.

17. Regarding Claims 23, 26 and 27 (incorrectly numbered 27 and 28), note Fig. 13 of Rho which shows the color filters formed on the insulating layer or second panel as recited to thus meet these claims.

18. Regarding Claims 24 and 25, note Fig. 8 of Okamoto which shows the color filters formed on the first panel as recited to thus meet these claims.

19. The choice of the first or second panel location for the color filters is deemed a matter of design expedient for the skilled worker in the liquid crystal art outside of any unobvious result produced thereby under 35 USC 103.

Conclusion

20. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JOHN HEYMAN whose telephone number is (571)272-5730. The examiner can normally be reached on 7:30am - 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571- 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. H./
Examiner, Art Unit 2871

/David Nelms/
Supervisory Patent Examiner, Art Unit 2871